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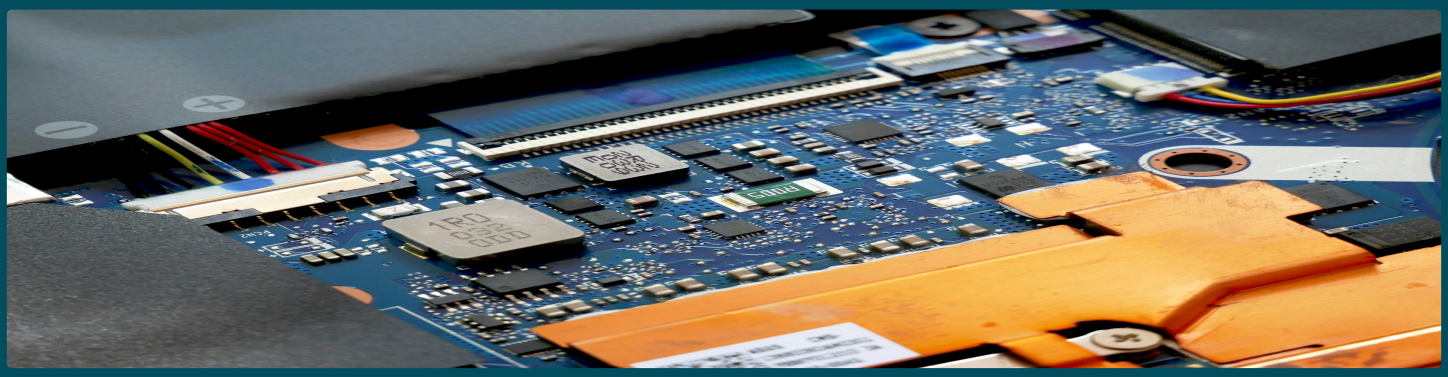

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IP Insights: How The DLI Scheme Is Shaping India’s Semiconductor IP Ecosystem

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Introduction

The Government of India, through the Ministry of Electronics and Information Technology (MeitY), continues to strengthen India's semiconductor ecosystem under the Semicon India Programme. A key pillar of this initiative is the Design Linked Incentive (DLI) Scheme, which directly targets the creation, ownership, and commercialization of semiconductor intellectual property (IP) within India.

From an intellectual property law perspective, the DLI Scheme is a significant policy intervention, as it prioritizes domestic generation of high-value chip design IP, encourages patent filings, and reduces India's dependence on foreign proprietary semiconductor technologies.

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Policy Background: Why Semiconductor Design IP Matters

Semiconductor design constitutes the most IP-intensive segment of the chip value chain. Unlike fabrication, which is capital-heavy, design focuses on:

- Integrated Circuit (IC) layouts
- System-on-Chip (SoC) architectures
- Embedded IP cores
- EDA-driven innovation

Ownership of these design elements determines market control, licensing power, and long-term technological sovereignty. Recognizing this, the DLI Scheme seeks to ensure that IP generated with public support remains anchored in India, aligning innovation policy with intellectual property protection.

Legal Structure of the DLI Scheme

India's semiconductor ecosystem is strengthened through a coordinated framework integrating policy leadership, financial incentives, capacity building, and indigenous technology development, supporting end-to-end chip design and commercialization.

Ministry of Electronics and Information Technology (MeitY):

- Provides national policy direction and anchors semiconductor initiatives.
- Coordinates industry and academic partnerships to strengthen the chip design and manufacturing ecosystem.

- Launched the Design Linked Incentive (DLI) Scheme to address structural challenges in domestic semiconductor design, helping Indian companies move up the semiconductor value chain.

Semicon India Programme (SIM):

- Allocated ?76,000 crore to support semiconductor and display manufacturing as well as the design ecosystem.
- Ensures end-to-end support for chip design, fabrication, and productization.
- The DLI Scheme operates under SIM, with C-DAC as the nodal implementing agency.

Chips to Startup (C2S) Programme:

- Umbrella capacity-building initiative implemented at academic institutions across India.
- Aims to generate 85,000 industry-ready professionals at B.Tech, M.Tech, and PhD levels in semiconductor chip design, bridging the skill gap in the sector.

Microprocessor Development Programme:

- Led by C-DAC, IIT Madras, and IIT Bombay.
- Designed, developed, and fabricated open-source microprocessors, including VEGA12, SHAKTI13, and AJIT, advancing India's self-reliance in critical technologies.

This institutional structure ensures that IP creation is supported not merely through funding, but also through state-facilitated access to design tools and prototyping infrastructure.

Eligibility Criteria and IP Ownership Considerations

Eligible Applicants

The Scheme is open to:

- DPIIT-recognized startups
- MSMEs
- Domestic companies meeting Indian ownership criteria

From an IP standpoint, this ensures that core design IP, patents, and trade secrets are generated by Indian entities, reducing risks of IP flight or foreign dominance.

IP Ownership Framework

While beneficiaries retain ownership of the IP they develop, the Scheme typically requires:

- Disclosure of milestones
- Reporting on IP generation (patents, layouts, copyrights)
- Compliance with contractual obligations regarding usage of government-supported infrastructure

This creates a balance between private IP rights and public accountability.

Incentives and Their IP Implications

Incentive Type	Description	Reimbursement/Cap Details
Product Design Linked Incentive (P-DLI)	Reimburses eligible costs for design, testing, and validation of ICs, SoCs, chipsets, systems, and IP cores.	Up to 50% of eligible expenditure, capped at ?15 crore per application.
Deployment Linked Incentive (DLI)	Provides incentives on net sales turnover when designs are deployed in electronic products.	4-6% of net sales over 5 years (min. cumulative net sales Years 1–5: ?1 crore for startups/MSMEs, ?5 crore for other domestic companies), capped at ?30 crore per application

Design Infrastructure and IP Governance

Support Type	Description
National EDA Tool Grid	Remote access to centralized advanced EDA tools for chip design activities.
IP Core Repository	Flexible access to repository of IP Cores for SoC design activities.
MPW Prototyping Support	Fiscal support for fabricating the design in MPW manner at semiconductor foundries.
Post-Silicon Validation Support	Fiscal support for testing, validation of fabricated ASICs, and silicon bring-up activities.

IP Outcomes and Early Indicators

Since its 2021 launch, the Design Linked Incentive (DLI) Scheme has significantly advanced India's semiconductor design ecosystem.

Major Milestones

- Sanctioned 24 chip-design projects across surveillance, drones, energy meters, microprocessors, and IoT SoCs.
- Enabled 16 tape-outs, 6 chip fabrications, 10 patents, and 140+ reusable IP cores.
- Supported 95 companies with EDA access (54M+ hours) and trained 1,000+ engineers.

These outcomes indicate that the Scheme is not merely subsidizing activity, but actively contributing to India's patentable semiconductor IP portfolio.

Success Stories Under India's Design Linked Incentive (DLI) Scheme

Several beneficiary companies have emerged as leading examples of how the DLI Scheme is translating indigenous design capability into silicon-proven, market-ready semiconductor products.

Vervesemi Microelectronics: Vervesemi has built a strong portfolio of 110+ semiconductor IPs, 25 IC variants, 10 granted patents, and 5 trade secrets, focusing on motor-control chips for BLDC motors used in consumer appliances, drones, and electric mobility.

InCore Semiconductors: InCore is developing indigenous RISC-V microprocessor IPs and SoC design automation tools, with its flagship Dolomite processor targeting entry-level smartphones and edge-AI applications. Its silicon-proven IP cores span fabrication nodes from 180 nm to 16 nm, reducing reliance on imported CPU IP.

Netrasemi: Netrasemi has successfully taped out India's first indigenously designed AI SoC on an advanced 12 nm node, integrating in-house AI/ML accelerators, vision processing and Video engines. The company has secured record private funding and plans multiple tape-outs across surveillance SoC variants.

Aheesa Digital Innovations: Aheesa is developing Vihaan, an indigenous fiber-broadband solution built on a VEGA processor–based Gigabit Passive Optical Network **(**GPON) ONT and Network SoC, enabling secure and cost-effective broadband connectivity. Reference platforms are expected to be introduced in 2026.

AAGYAVISION: AAGYAVISION is designing all-weather radar-on-chip solutions driving advancements in safety, security, smart infrastructure, edge computing, and emerging 6G sensor networks, and also for critical use cases such as drone detection.

Collectively, these success stories demonstrate how the DLI Scheme is converting indigenous chip design capabilities into commercially viable, silicon-proven products. By supporting advanced design, prototyping, and commercialization, the Scheme is strengthening India's technological self-reliance and reinforcing its position within the global semiconductor design ecosystem.

Conclusion: A Strategic Shift Toward IP-Led Semiconductor Growth

The Design Linked Incentive (DLI) Scheme is a targeted policy instrument aimed at strengthening India's fabless semiconductor design ecosystem by incentivising the creation, ownership, and commercialization of indigenous semiconductor intellectual property (IP). By combining financial support, access to advanced design infrastructure, and a structured institutional framework, the Scheme directly benefits Indian startups, MSMEs, domestic companies, and research institutions engaged in chip design. It lowers entry barriers, mitigates early-stage financial risk, and enables innovators to translate design capabilities into silicon-proven, market-ready products. In doing so, the DLI Scheme advances India's objectives of technological self-reliance, reduced dependence on foreign IP, and long-term competitiveness in the global semiconductor value chain.

For more details, write to us at: contact@indialaw.in

Reference:

1. https://www.pib.gov.in/PressReleseDetailm.aspx?PRID=2211220&reg=3&lang=2

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